

IN THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 21, as follows.

The present invention is related to United States Patent Application Number 09/788,582, entitled "Method and Apparatus for Transferring Multi-Source/Multi-Sink Control Signals Using a Differential Signaling Technique," (~~Attorney Docket Number Fernando 9-11-4~~),
 5 United States Patent Application Number 09/785,602, entitled "Method and Apparatus for Distributing Multi-Source/Multi-Sink Control Signals Among Nodes on a Chip," (~~Attorney Docket Number Fernando 10-12-5~~), United States Patent Application Number 09/785,653,
 entitled "Bidirectional Bus Repeater for Communications on a Chip," (~~Attorney Docket Number Hunter 4-13-4~~) and United States Patent Application Number 09/785,592, entitled "On-Chip
 10 Method and Apparatus for Transmission of Multiple Bits Using Quantized Voltage Levels," (~~Attorney Docket Number Lee 15-6~~), each filed contemporaneously herewith, assigned to the assignee of the present invention and incorporated by reference herein.

Please amend the paragraph beginning at page 1, line 21, as follows.

As the clock frequency increases at which integrated circuits operate, the clock period decreases such that there is less time available to accommodate integrated circuit trace propagation delays in the clock signal. A high frequency clock signal is typically generated by a clock generation circuit using a low frequency crystal as a reference clock signal. The clock
 20 generation circuit includes a frequency synthesizer to produce the high frequency clock signal output. The high frequency clock signal is routed through traces on an integrated circuit to devices such as a cache controller, processors, and random access memories. It is desirable to have clock signals arrive at all devices at precisely controlled times, which may be or may not be simultaneous. The devices receiving the clock signal are located at various distances from the
 25 clock generation circuit resulting in traces of different length over which the clock signal must propagate.